A UHF BAND 1.3W MONOLITHIC AMPLIFIER WITH EFFICIENCY OF 63%

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ABSTRACT

A UHF band 1.3W 4-stage monolithic amplifier with an efficiency of 63% has been developed for transmitters of mobile communications. To obtain a high efficiency, a novel miniaturized second harmonic terminating circuit was devised, having a parallel resonant circuit comprised of lumped elements. The size of the amplifier is 8.6 X 5.8mm.

INTRODUCTION

Optimally loaded and overdriven RF power amplifiers[1,2,3,4] are very useful for transmitters of mobile communications because of high efficiency characteristics. In the amplifiers, to obtain high efficiency, even and odd harmonic waves have been terminated in a short and an open circuits, respectively[1]. In most of the conventional power amplifiers with high efficiency, a 1/4-wavelength short stub[2] or a 1/8-wavelength open stub[3] at the fundamental frequency is utilized to make a short circuit for even harmonic waves. However, wavelength becomes so long in the UHF band that their sizes become large. From the point of view that the second harmonic wave has a predominant effect on the efficiency of high power amplifiers, we devised a novel miniaturized second harmonic terminating circuit with a parallel resonant circuit comprised of lumped elements. The parallel resonant circuit becomes an open circuit at the second harmonic wave. With the use of the novel second harmonic terminating circuit, a 4-stage monolithic power amplifier has been developed. A maximum drain efficiency of 63% has been obtained with a saturated output power higher than 31dBm in the UHF band. The size of the amplifier is 8.6 X 5.8mm.

CIRCUIT DESIGN

For the design of a high efficiency power amplifier, we measured the load conditions providing a maximum output power and the load conditions providing a maximum drain efficiency. The load conditions for the fundamental and the second harmonic waves were measured with the use of a conventional load-pull and an active second harmonic load-pull[5], respectively.

Fig.1 shows a measurement set-up of the active second harmonic load-pull. The second harmonic wave generated by a frequency doubler is tuned by a phase shifter and a variable attenuator, and is injected to a FET under test through a broadband circulator and an output matching circuit. This method has an advantage in that the load condition for the second harmonic wave can be varied without affecting the load condition for the fundamental wave. Fig.2(a) shows output power versus $\angle\Gamma_x$ for three values of $|\Gamma_x|^2$, where Γ_x is the load reflection coefficient for the second harmonic wave. The FET under test has a gate width of 3.18mm and is matched to 50 Ω at the fundamental frequency. It is clear from Fig.2(a) that the output power changes by injecting second harmonic wave and that the maximum output power is 27.6dBm for the condition of $\angle\Gamma_x = -70°$ and $|\Gamma_x|^2 = 0$dB, which is realizable by using passive circuit elements. Fig.2(b) shows power-added efficiency versus $\angle\Gamma_x$. From Fig.2(b), the maximum power-added efficiency is 74.2% for the same condition.

Fig.3 shows a measurement set-up of the load-pull for the fundamental wave. A second harmonic reflection circuit is located between a FET under test and a tuner. So, this method has an advantage in that the load conditions for the fundamental wave can be varied without affecting the load conditions for the second harmonic wave. Fig.4 shows output power and drain efficiency for various values of the load impedance for the fundamental wave under the condition that the load impedance for the second harmonic wave is adjusted to the condition that the drain efficiency becomes maximum. The FET under test has a gate width of 7.28mm and the measurement was done at 920MHz. From Fig.4, a maximum output power of 32.2dBm was obtained, when the drain efficiency was 59.8%.

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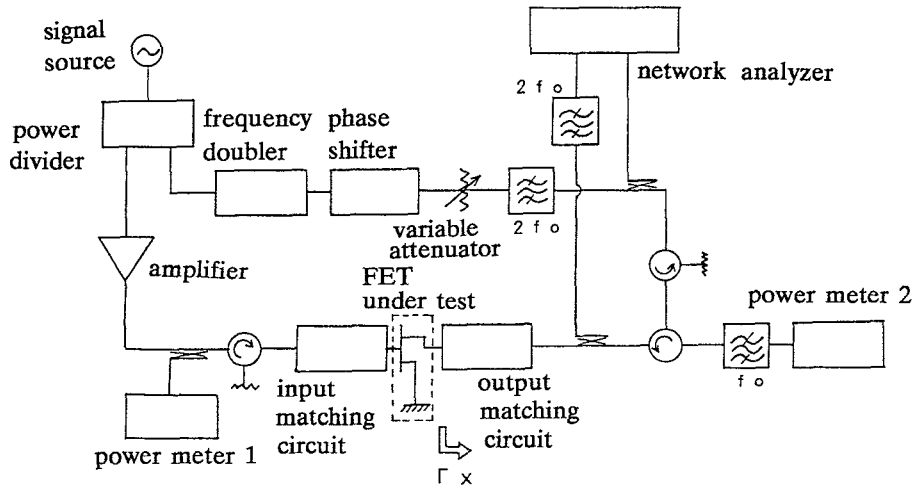
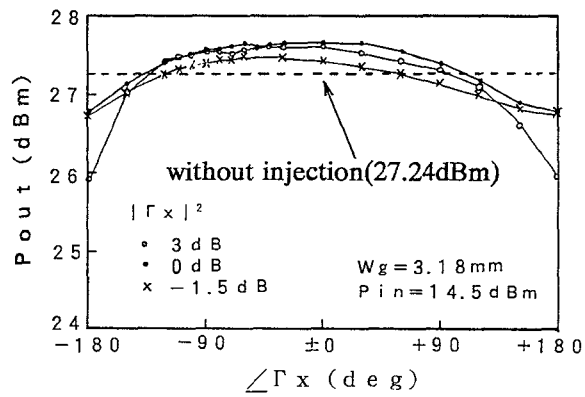
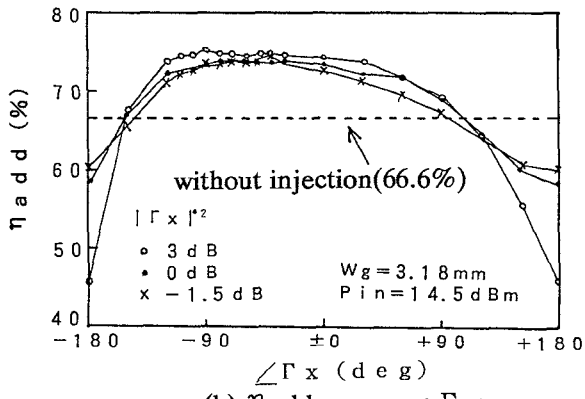


Fig.1 Measurement set–up of the active second harmonic load–pull.



(a) Pout versus ∠ Γ x



(b) η add versus ∠ Γ x

Fig.2 Output power (Pout), power added efficiency (η add) versus Γx characteristics measured by the active second harmonic load–pull.

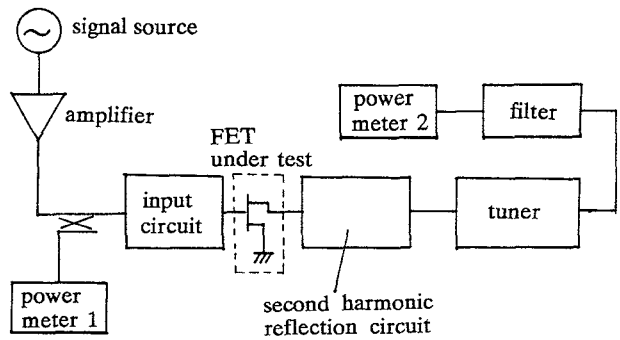


Fig.3 Measurement set–up of the load–pull for the fundamental wave.

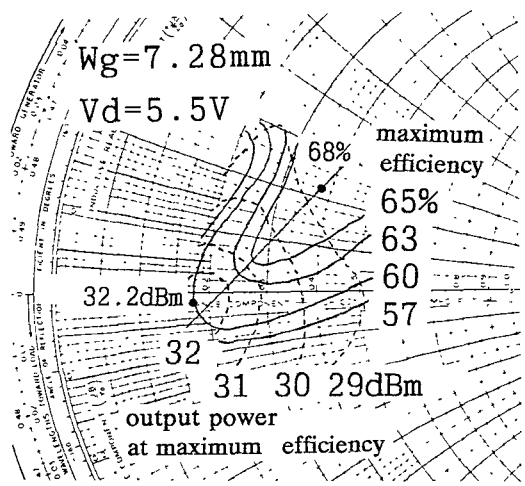


Fig.4 Experimental results of the load–pull for the fundamental wave.

On the other hand, a maximum drain efficiency of 68.2% was obtained, when the output power was 28.4dBm.

Based on the measured data for the fundamental and the second harmonic waves, a 4-stage monolithic power amplifier with a novel second harmonic terminating circuit has been designed.

Fig.5 shows a schematic diagram of the amplifier. The number of amplifier stages was determined to be four to get a large signal gain greater than 40dB and the gate width of the final stage FET was determined to be 7.28 mm to get a saturated output power higher than 31dBm from the results of Fig.4. The final stage FET is optimally loaded for the second harmonic wave by using a devised second harmonic terminating circuit which is made of a phase-adjusting transmission line and a parallel resonant circuit comprised of lumped elements. The parallel resonant circuit becomes an open circuit, and the phase-adjusting transmission line makes an optimum load reflection coefficient for the second harmonic wave. Moreover, this amplifier employs a quarter-wave open stub for the third harmonic wave in the output matching circuit to prevent the third harmonic dissipation.

From Fig.4, the load condition for the fundamental wave was designed to be $Z=13+j2.5\ \Omega$ at 920MHz, where the second harmonic terminating circuit was designed to be a reflection coefficient of $\angle\Gamma_x=-120^\circ$ and $|\Gamma_x|^2=0$dB.

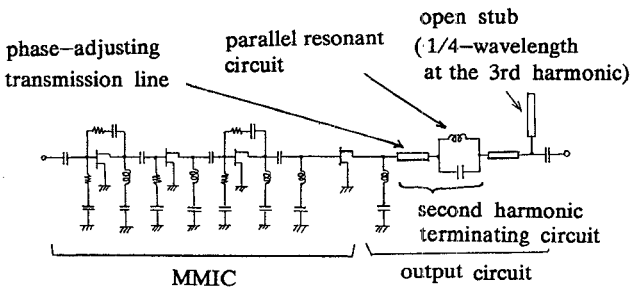


Fig.5 Schematic diagram of 4-stage monolithic power amplifier with a novel second harmonic terminating circuit.

EXPERIMENTAL RESULTS

Fig.6 shows a photograph of the 4-stage monolithic power amplifier. The output matching circuit of the final stage amplifier was fabricated on an alumina substrate to reduce a circuit loss and to achieve a higher output power and efficiency. The other circuit was fabricated on GaAs substrates. The overall circuit size is 8.6 X 5.8mm.

Fig.7 shows a measured output power of the amplifier. The saturated output power is higher than 31dBm for the frequency range from 840MHz to 1GHz at a bias condition of Vd=5.5V and Idso=0.1 Idss (deep "class AB" operation). Fig.8 shows a measured drain efficiency of the amplifier at 920MHz. The measured maximum drain efficiency is 63% at 31.2dBm output power. Fig.9 shows measured harmonic levels of the amplifier relative to the fundamental level. The second and third harmonics are kept below −50dBc and −40dBc, respectively. Fig.10 shows predicted and measured small signal gains of the amplifier. They are in good agreement. The measured small signal gain is higher than 50dB for the frequency range from 840MHz to 1GHz.

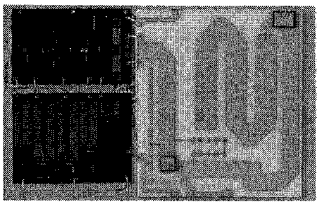


Fig.6 The potograph of 4-stage monolithic power amplifier.

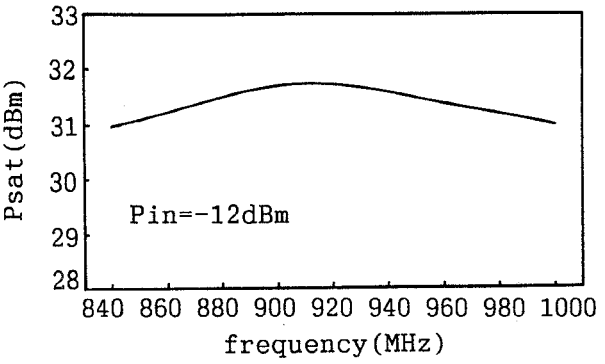


Fig.7 Saturated output power (Psat).

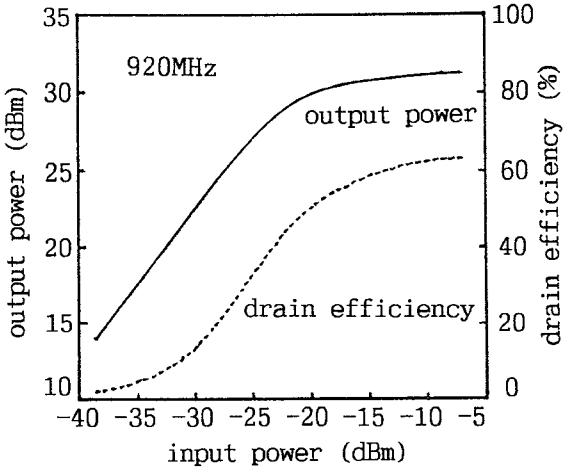


Fig.8 Output power, drain efficiency.

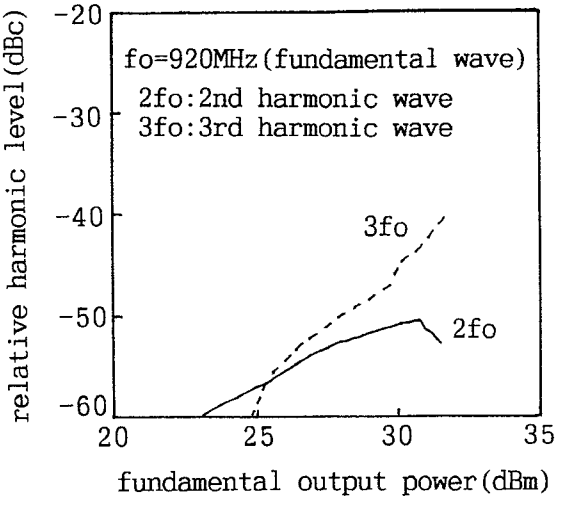


Fig.9 Harmonic levels.

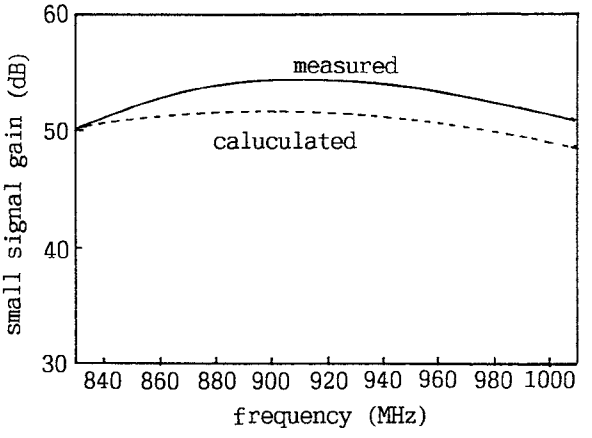


Fig.10 Small signal gain.

CONCLUSION

A UHF band high efficiency, 4–stage monolithic power amplifier with a novel miniaturized second harmonic terminating circuit has been developed. With the use of a parallel resonant circuit comprised of lumped elements for terminating the second harmonic, it achieves a maximum drain efficiency of 63%, a saturated output power of higher than 31dBm in the UHF band, and occupies an area of 8.6 X 5.8mm.

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